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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/822,730	04/13/2004	Shinobu Nohtomi	XA-10079	2939

181 7590 03/12/2007

MILES & STOCKBRIDGE PC
1751 PINNACLE DRIVE
SUITE 500
MCLEAN, VA 22102-3833

EXAMINER	
KARIMI, PEGEMAN	
ART UNIT	PAPER NUMBER
2609	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/12/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/822,730	NOHTOMI ET AL.	
	Examiner	Art Unit	
	Pegeman Karimi	2609	

– The MAILING DATE of this communication appears on the cover sheet with the correspondence address –

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 April 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☒ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. Acknowledgment is made of applicant's claim for foreign priority based on an application filed in 10/822,730 on 04/13/2004. It is noted, however, that applicant has not filed a certified copy of the foreign priority documents as required by 35 U.S.C. 119(b).

2. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Drawings

3. Figures 11-13 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-4, 6-8, 10, 12-14, 16, and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kanatani (U.S. Patent 5,414,443), and in view of Sakaguchi (U.S. Patent 7,006,114).

As to claim 1, Kanatani discloses a liquid crystal drive method comprising a circuit (2) having a plurality of gradation voltages ($V_0 - V_{15}$) to be given to a pixel electrode (103) of a liquid crystal and a common voltage (Vc) given to a common electrode (105) of the liquid crystal in which said common voltage is switched between a positive phase and a negative phase (col. 10, lines 5-7),

Kanatani teaches a first voltage (e.g. $+V_3$ to $+V_7$) is applied as said gradation voltage in the positive phase of said common voltage, a second voltage (e.g. $-V_3$ to $-V_7$) is applied as said gradation voltage in the negative phase of said common voltage (See Fig. 17a – 17b, and col. 10, lines 2-15), said first voltage and said second voltage are opposite in polarity with reference to a voltage (Va) of the common electrode, Kanatani does not teach first and second voltages selected from first and second display data,

where in the first and second display data are the same bit pattern except for one specific bit.

Sakaguchi teaches a first voltage (e.g. $+V_{32}$ to $+V_{63}$) is selected from first display data (Table 1, 20H – 3FH), and said second voltage (e.g. $-V_{32}$ to $-V_{63}$) is selected from second display data (Table 1, 00H-1FH), wherein said first display data and said second display data are obtained by converting display data from outside (col. 9, lines 9-10), and when said first and second display data are the same, said first display data and said second display data are in the same bit pattern except for one specified bit (i.e. the bit pattern in low level '0' are the same bit pattern in high level '1' except the most significant bit "MSB" (see table 1 of col. 17)). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to have provided the digital display data for selecting gradation voltage of Sakaguchi to the gradation voltages of Kanatani because the display data for selecting gradation voltages of Sakaguchi would provide reduction in power consumption of the driving circuit and miniaturization of a driving circuit (see col. 16, lines 1-8 of sakaguchi)

As to claim 2, Sakaguchi teaches that one specified bit being the highest order bit (most significant bit), (see col. 17, table 1).

As to claim 3, Sakaguchi teaches when a positive-negative switch signal of said positive phase and negative phase (col. 13, lines 19-37) is at a level corresponding to logic 0 (col. 13, line 30), the highest order bits (Table 1, Most significant bit) of said first

display data (table 1, 20H – 3FH) and second display data (Table 1, 00H – 1FH) are allocated as they are (col. 13, lines 29-32), respectively, and when said positive-negative switch signal is at a level corresponding to logic 1 (col. 13, line 35), the highest order bits (Table 1, Most significant bit) of said first display data and said second display data are inverted and allocated (col. 13, lines 34-38) , respectively,

when said highest order bits (Table 1, MSB) are at a level corresponding to logic 1 (col. 16, lines 12-13), data of the second order ($V_{32} - V_{63}$, col. 16, lines 14-15) and lower bits (Table 1, bit 0 – bit 4) of said first display data and second display data are allocated as they are (col. 13, lines 29-32), and when said highest order bits are at a level corresponding to logic 0 (col. 16, line 20) , the second order ($V_0 - V_{31}$, col. 16, line 22) and lower bits (Table 1, bit 0 – bit 4) of said first display data (20H – 3FH) and second display data (00H – 1FH) are inverted and allocated (col. 13, line 37) .

As to claim 4, Sakaguchi (Fig. 1) teaches a circuit (12) outputs display data (Table 1, 00H-3FH) from an incorporated memory (33) writing and reading said display data to be displayed on a liquid crystal panel (col. 2, lines 18-22), and display data is converted (col. 6, lines 18-20) by a display data conversion circuit (371 & 372) to said first display data and second display data, respectively, by control of the positive-negative switch signal (col. 6, lines12-24).

As to claim 6, Kanatani discloses a liquid crystal display system (1 and 100) comprising:

a liquid crystal display panel (100) having a signal line (102) supplying a gradation voltage to a pixel electrode (103),

a scanning line (101) selecting the pixel electrode, and a common electrode (105) opposite said pixel electrode (col. 13, lines 1-4, and lines 6-9); a liquid crystal drive voltage generation circuit (2) generating a plurality of gradation voltages for gradation display (col. 12, lines 41-43).

a segment driver (2) including an output gradation selector (55) selecting any one of said plurality of gradation voltages ($V_0 - V_{15}$) according to display image data to output the gradation voltage to the signal line of said liquid crystal display panel (100), (col. 10, lines 10-15);

a gate driver (300) outputting a select signal sequentially selecting the scanning line of said liquid crystal display panel (100) according to a display timing signal (col. 1, lines 51-55); and

a common electrode drive circuit (8; see fig. 12) switching a common voltage (Vc) given to the common electrode (105) of said liquid crystal display panel (100) by a positive-negative switch signal corresponding to a positive phase and a negative phase (AC-driven), (col. 12, lines 58-62), wherein said common electrode drive circuit (8) switches said common voltage (Vc) between said positive phase and negative phase (AC-driven), (col. 12, lines 60-62).

Sakaguchi (Fig. 1) teaches an output gradation selector (36 and 39) receives, as an input, first display data in the positive phase (first positive amplitude) of said common voltage (fig. 17 b, first negative amplitude), outputs a signal selecting a first voltage as

said gradation voltage corresponding to said first display data to said liquid crystal drive voltage generation circuit (Fig. 17 c, transmittance), receives, as an input, second display data in the negative phase, of said common voltage, and outputs a signal selecting a second voltage as said gradation voltage corresponding to said second display data to said liquid crystal drive voltage generation circuit,

a first display data and said second display data are obtained by converting display data from outside (col. 9, lines 9-10), and there is provided a display data conversion circuit (12) that converts for output (col. 9, lines 14-16), to said first display data and said second display data display data to be displayed on said liquid crystal display panel (col. 11, lines 16-19) so that other bits are the same (bit 0 – bit 4) except for one specified bit (MSB) when said first and second display data are the same (Table 1, bit 0 – bit 4).

As to claim 12, this claim differs from claim 6 only in that the limitations state a liquid crystal drive control device (1 and 100) comprising: a liquid crystal drive voltage generation circuit (2) generating a plurality of gradation voltages for gradation display (col. 12, lines 41-43).

As to claim 18, the limitation "control device, which is manufactured over one semiconductor substrate" is well known in the art.

As to claims 7 and 13, Sakaguchi teaches one specified bit (Table 1, MSB) is the highest order bit (Table 1, bit 5), and wherein said display data conversion circuit (37) outputs (col. 13, lines 29-32) the highest order bits (Table 1, MSB) of display data (Table 1) as they are when a positive-negative (col. 13, lines 19-23) switch signal (col. 13, line 19) of said positive phase and negative phase (col. 13, lines 15-18) is at a level corresponding to logic 0 (col. 13, line 30), inverts and outputs (col. 13, lines 36-38) the highest order bits (Table 1, MSB) of said display data when said positive-negative (col. 13, lines 19-23) switch signal (col. 13, line 19) is at a level corresponding to logic 1 (col. 13, line 35), thereby forming the highest order bits of said first display data and second display data, outputs data of the second order ($V_0 - V_{31}$, col. 16, line 22) and lower bits (Table 1, bit 0 to bit 4) of said first display data and second display data as they are (col. 13, line 32) when said highest order bits are at a level corresponding to logic 1 (col. 13, line 30), and outputs inverted (col. 13, line 37) data of the second order (col. 13, line 37) and lower bits (Table 1, bit 0 – bit 4) of said first display data and second display data when said highest order bits are at a level corresponding to logic 0 (col. 13, line 35).

As to claim 8 and 14, Kanatani (Fig. 2) teaches a first display data and second display data are transmitted (col. 8, lines 56-58) to a decoder circuit (40) having a low voltage amplitude (Fig. 2, Vcc-Vss = +5v) corresponding to a logic circuit (col. 9, lines 12-15), an output signal (col. 8, line 58) of the decoder circuit is transmitted to a level shifter circuit (60) shifting a signal of said low voltage amplitude (Vcc-Vss = +5V) to a signal of a high voltage amplitude (Vcc – Vdd = +15V), and an output signal of the level

shifter circuit is decoded (50) to form a select signal selecting said gradation voltage (col. 12, lines 48-53).

As to claim 10 and 16, Sakaguchi (Fig. 2) teaches a segment driver (12) has an incorporated memory (33) writing and reading said display data (Table 1, 00H-3FH) to be displayed on said liquid crystal panel (col. 2, lines 18-22), and wherein said display data conversion circuit (371 and 372) converts said display data outputted from said incorporated memory (33) to said first display data and second display data, respectively, by a positive-negative switch signal (col. 6, lines 12-24).

6. Claims 5,11, 17,19, 20, and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kanatani (U.S. Patent 5,414,443), and in view of Sakaguchi (U.S. Patent 7,006,114) as applied to claim 1 above, and further in view of Chang (U.S. Patent 6,611,247).

As to claims 5, 11, 17, 19, and 20-21, note the discussion of Kanatani and Sakaguchi above. Both do not teach a microprocessor unit for generating a display data. Chang (Fig. 1) teaches a display data is given by a microprocessing unit (70) for generating said display data (col. 3, lines 46-49). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to have provided the controller for converting a digital signal of either logic '0' or '1' into multi-level data signals of Kanatani to the gradation voltage of Sakaguchi because the controller for

converting a digital signal into multi-level data signal of Kanatani would provide width of the multi-level signal bus to be reduced (col. 3, lines 54-59).

7. Claims 9 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kanatani (U.S. patent 5,414,443), in view of Sakaguchi (U.S. Patent 7,006,114) as applied to claim 1 above, and further in view of Pappalardo (Pub. No. 2005/0219191).

As to claims 9 and 15, Kanatani and Sakaguchi do not teach a boost voltage and a charge pump. Pappalardo (Fig. 5) teaches an operation voltage (paragraph 28, lines 4-5) of said level shifter circuit (11 and 12) is a boost voltage (paragraph 28, line 7) formed by a charge pump circuit (paragraph 28, line 8). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to have used the boost voltage of Pappalardo to the liquid crystal of Kanatani as modified by Sakaguchi because the boost voltage increases the voltages of logic signals from a low level to a higher level for different applications within the device. (paragraph 9)

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Monomohshi (Pub. No. 2004/0104874) discloses a liquid crystal driving device.

Inquiries

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Pegeman Karimi whose telephone number is (571) 270-1712. The examiner can normally be reached on Monday-Thursday 8:00am - 5:00pm EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chanh Nguyen can be reached on (571) 272-7772. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

02/27/2007
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